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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GOSSAGE, GLENN A	

ART UNIT	PAPER NUMBER
2187	11

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/731,788	SUKEGAWA, HIROSHI	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,8,9,13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,8,9,13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *16 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. It appears "SELECTIVELY CONTROLLED" should be changed to --PLURAL--, and --SELECTIVELY CONTROLLED BY A MASTER CHIP ENABLE TERMINAL OR AN INPUT COMMAND AND OUTPUTTING A PASS/FAIL RESULT-- or other similar language inserted after "CIRCUITS" for clarity and completeness (see claim 1, lines 1-3 and 8; claim 9, lines 1-2 and 6; and claim 13, lines 1-3 and 6, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

2. The abstract of the disclosure is objected to because in line 3, it appears "Electronically" should be --Electrically-- for clarity and consistency (note the change made in the paragraph beginning on page 1, line 11, e.g.).

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on June 16, 2003 have been approved by the Examiner, subject to drafting review. [The drawings would not appear to be formal drawings since many of the lines are jagged and unclear (not sufficiently darkened). Compare the originally filed drawings, for example.]

Corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

4. It is once again noted that this application appears to contain claims directed to different inventions or different species of the same invention (here, an electrically rewritable nonvolatile semiconductor memory device). More specifically, the application contains claims (see claims 1, 4-6, 8, 15 and 18, e.g.) directed to an electrically rewritable nonvolatile semiconductor memory device including control circuits for sequentially controlling writing and, in various embodiments, a chip enable terminal or an inputted command for controlling the inactivity and inactivity of the memory circuits. Other claims (see claims 9, 13, 16-17 and 19-20, e.g.) are directed to an electrically rewritable nonvolatile semiconductor memory device including plural memory circuits, each having at least one stage of a data buffer, writing operations being simultaneously carried out via the data buffer, and in which pass/fail results are outputted or accumulated.

While these inventions or species appear to be distinct, a restriction requirement is NOT being made at this time since it does not appear there will be a substantial burden on the Office if restriction is not required. However, restriction may be required in the future depending on how the claims are amended.

5. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

In the paragraph beginning on page 1, line 26, at line 6 of the paragraph, it appears "6-95125 and 6-95126" should be changed to --07-302175 and 07-302176-- for clarity (note that these are publication numbers, not application numbers).

In the paragraph beginning on page 2, line 8, at line 1 of the paragraph, it appears "CPU" should be changed to --(CPU)-- for clarity.

In the paragraph beginning on page 3, line 14, at line 2 of the paragraph, it appears "plurality" should be --plural-- for clarity. [Note that the amendment to the paragraph referring to Figure 2 and purportedly beginning on page 3, line 14 (at the bottom of page 3 of the amendment) has NOT been entered (note the amendment to the paragraph beginning on page 3, line 34 at the top of page 4 of the amendment).]

In the paragraph beginning on page 4, line 28, at line 6 of the paragraph, it appears "I/O buffer, 26" should be changed to --(I/O) buffer, -- for clarity.

In the paragraph beginning on page 5, line 2, at line 10 of the paragraph, the proper antecedent for "These signals" is not adequately clear here. [Are the enable signals also input to control circuit 29 in Fig. 2?]

In the paragraph beginning on page 5, line 22, at lines 9-10 of the paragraph, it appears "by small unit of storage capacitor" should be changed to --data for every small unit of storage capacity-- for clarity and consistency with the disclosure as originally filed.

In the paragraph beginning on page 7, line 18, at line 1 of the paragraph, it appears "a" should be --the--.

In the paragraph beginning on page 7, line 28, at line 5 of the paragraph, it appears "generation" should be --generations--.

In the paragraph beginning on page 7, line 35, at lines 1-2 of the paragraph, it is not clear what is meant by "the control is not often continued," particularly when read in light of the language of the specification as originally filed at page 7, lines 35-36 ("a little control continues to enter each of the EEPROM circuits?"). Clarification by way of amendment and/or explanation is required.

In the paragraph beginning on page 8, line 27, at line 6 of the paragraph, it appears "at a time" should be --at one time--, and "one high-speed operation" changed to --a high-speed operation--, for clarity.

In the paragraph beginning on page 9, line 11, at lines 11-12 of the paragraph (page 9, lines 21-22), the language "Each of the EEPROM circuits 2 does not include any control circuits" is unclear and confusing when read in conjunction with lines 17-19. That is, if "commands, addresses and data (are allowed) to be inputted to the I/O buffer of each of the EEPROM circuits" as stated in lines 17-19, it would appear the EEPROM circuits would contain some "control circuits."

In the paragraph beginning on page 11, line 4, at line 7 of the paragraph, it appears "input In" should be --input. In-- for clarity.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 5, line 2, it appears "comprising a" should be --comprising: a-- (i.e., a colon should be added and a new sub-paragraph started similar to claim 1, lines 2-3) for clarity and consistency. See also claim 9, line 2.

Appropriate correction is required.

6. Claims 1, 4, 9, 13 and 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, and therefore its dependent claims, it is not clear how the activity and inactivity of each of the memory circuits is controlled "by a logical output of a signal of said master chip enable terminal" as the dependence on the chip enable terminals is not clear (compare the language of original claim 3, lines 4-7, e.g.). [Should language such as --and a respective chip enable terminal-- be inserted after "terminal" in line 10?]

In claim 9, and therefore its dependent claims, it is not entirely clear to where the at least one data buffer stage "transmits" the data (see line 4, e.g.). [Should "transmitting" in line 4 simply be changed to --storing--? Note lines 7-8, e.g.] Claim 13 (line 4) is analogously unclear.

In claim 13, and therefore its dependent claims, lines 8+, the wording "wherein it is determined ... and a mode in which ..." is unclear and confusing. It appears language such as --said electrically rewritable nonvolatile semiconductor memory device has a mode in which-- should be (re)inserted after "wherein" in line 8 for clarity (note the language of original claims 13-14, lines 2-4, e.g.). In line 9, the proper antecedent for "said at least one data buffer stage" is not entirely clear since there are plural memory circuits, each having "at least one data buffer stage," set forth in the claims (see claim 13, lines 3-4). Similarly, the proper antecedent for "said pass/fail result" in lines 9 and 11 is not adequately clear since there are plural writing operations, each with a pass/fail result, set forth in the claims (see claim 13, line 6, e.g.). The proper antecedent for "said data buffer" in line 10 is analogously unclear (again note that there are plural memory circuits, each having "at least one data buffer stage," set forth in lines 3-4).

In claims 15-17, it is not clear how the "memory circuits (have) a stacked gate structure." It appears "has" in claims 15-17, line 2 should be changed to --includes memory cells having-- for clarity and consistency (see page 4, line 30 of the original specification, e.g.).

Similarly, in claims 18-20, it is not clear how the "stacked gate structure (of the memory circuits) is a stacked gate structure." It appears "stacked gate structure is" in claims 18-20, line 2 should be changed to --memory cells are arranged in-- for clarity and consistency (in conjunction

with the changes suggested above for claims 15-17. Note page 4, lines 30-31 of the original specification, e.g.).

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9 and 16, insofar as definite and clear, are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al.

With respect to claim 9, Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device such as an electrically erasable programmable read only memory (EEPROM) including a plurality of "memory circuits," provided in a memory chip, as in the present invention [see the EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 3, lines 15-17 and 55-58, e.g.]. Lee et al discloses that each of the memory circuits is provided with at least one stage of a "data buffer" [see data registers 404, 405, 409 and 410 in Figure 3 and column 4, lines 46-49, e.g.] for transmitting or storing writing data corresponding to the address, and also teaches that writing operations in the plurality of memory circuits may be simultaneously carried out "via" or using the data buffer in each of the memory

circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al also discloses that the "pass/fail" results of each of the writing operations may be ascertained by corresponding program/verify circuits (such as 454 and 460 in Figure 3) and outputted to each of the respective memory circuits.

With respect to claim 16, the memory cells in Lee et al use nonvolatile EEPROM transistors which have a "stacked gate" (floating gate and control gate) structure.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 15 and 18, as well as claim 19, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (U.S.'001) and Lee et al, taken together.

With respect to claim 1, Sukegawa et al ('001) discloses an electrically rewritable nonvolatile semiconductor memory device, such as an electrically erasable programmable read only memory (EEPROM), including a plurality of "memory circuits," each of which has a control circuit for sequentially controlling writing so as to share a data bus, as in the present invention. See EEPROM memory circuits 11-1 to 11-3 and 11-16 in Figure 2, as well as column 40, lines 55-65, e.g. Sukegawa et al (U.S. '001) also discloses a chip enable terminal provided for each of the

memory circuits, for controlling the activity and inactivity of each of the memory circuits [see the chip enable terminals CE and signals CS1 to CS3 and CS16 in Figure 2, as well as column 14, lines 33-51, e.g.]. Sukegawa et al (U.S. '001) also discloses that each of the memory circuits is provided with a ready/busy signal terminal which corresponds to a respective chip enable terminal [see the RDY/BUSY terminals in EEPROMs 11-1 to 11-3 and 11-16 and signals R/B1 to R/B3 and R/B16 in Figure 3, as well as column 14, lines 47-51 and column 18, lines 15-24, e.g.] However, Sukegawa et al does not teach that the plurality of memory circuits are "provided in a memory chip."

Lee et al similarly discloses an electrically rewritable semiconductor memory device such as an EEPROM including a plurality of "memory circuits" which share a data bus, and also teaches that writing operations in the plurality of memory circuits may be simultaneously carried out in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al also discloses providing a "master" enable signal or terminal for controlling the activity and inactivity of the plurality of memory circuits "as a whole," with the activity and inactivity of each of the memory circuits being controlled by "a logical output" of the "master" enable signal [see the logic in Figures 6, 8 and 9, particularly the AND logic in Figure 9 which outputs signals in response to a master program signal to control the "activity" and "inactivity" of circuitry within each of the memory circuits]. Lee et al also teaches that the plurality of memory circuits may be "provided in a memory chip" [see column 3, lines 15-17 and 55-58, e.g.] with each of the memory circuits including control or enable signals to allow individual control

of the writing operations in each of the memory circuits provided on the memory chip and coupled to the shared data bus [see EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 4, line 50 to column 5, line 7, e.g.]. As those of ordinary skill in the art would readily appreciate, integrating a plurality of similar circuits on an integrated circuit (IC) or "chip" allows the overall size and cost of the circuit to be decreased, and also provides fewer interconnections, increasing reliability.

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to provide the plurality of EEPROM memory circuits in Sukegawa et al (U.S. '001) "in a chip," with each of the memory circuits including individual control and enable signals, as taught by Lee et al, in order to allow a "time sharing" control of a data bus coupled to the plurality of memory circuits and allow writing operations to be carried out in parallel in each of the memory circuits. The reduction in access time and increase in operating speed obtained by performing the writing operations in parallel, coupled with the well known benefits of smaller overall size and cost, and improved reliability, obtained by integrating or providing a plurality of circuits such as memory circuits "in a chip," provides ample motivation and suggestion to provide the plurality of memory circuits in Sukegawa et al "in a chip."

Since applicant's claims "read on" a structure and method rendered obvious to one of ordinary skill in the art by the combined teachings of the references, the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the prior art.

With respect to claim 4, Lee et al also discloses controlling the activity and inactivity of each of the memory circuits by a logical output of the "master" enable signal and a signal of the chip enable terminal of each of the memory circuits [see the AND logic in Figures 6, 8 and 9, e.g., which outputs signals to respectively control the "activity" and "inactivity" of circuitry within each of the memory circuits].

With respect to claims 15 and 18, Sukegawa et al (U.S. '001) teaches using memory circuits or cells having a "stacked gate" (a floating gate and a control gate, e.g.), with the cells being arranged to form a NAND structure (see column 14, lines 29-53 of Sukegawa et al (U.S. '001), e.g.).

With respect to claim 19, Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device such as an electrically erasable programmable read only memory (EEPROM) including a plurality of "memory circuits," provided in a memory chip, as in the present invention [see the EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 3, lines 15-17 and 55-58, e.g.]. Lee et al discloses that each of the memory circuits is provided with at least one stage of a "data buffer" [see data registers 404, 405, 409 and 410 in Figure 3 and column 4, lines 46-49, e.g.] for transmitting or storing writing data

corresponding to the address, and also teaches that writing operations in the plurality of memory circuits may be simultaneously carried out "via" or using the data buffer in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al also discloses that the "pass/fail" results of each of the writing operations may be ascertained by corresponding program/verify circuits (such as 454 and 460 in Figure 3) and outputted to each of the respective memory circuits. As one of ordinary skill in the art would readily appreciate, the memory cells in Lee et al utilize nonvolatile EEPROM transistors which have a "stacked gate" (floating gate and control gate) structure. While a NAND type EEPROM is not specifically discussed, the use of a well known NAND type EEPROM such as taught by Sukegawa et al (U.S. '001) in order to provide improved integration density by using serially connected EEPROM transistors would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not render the claimed invention patentably distinct.

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (U.S.'001) and Lee et al, taken together.

With respect to claim 5, Sukegawa et al ('001) discloses an electrically rewritable nonvolatile semiconductor memory device, such as an electrically erasable programmable read only memory (EEPROM), including a plurality of "memory circuits," each of which has a control circuit for sequentially controlling writing so as to share a data bus, as in the present invention (see

EEPROM memory circuits 11-1 to 11-3 and 11-16 in Figure 2, as well as column 40, lines 55-65, e.g.). Sukegawa et al ('001) also generally discusses that the "activity" and "inactivity" of each of the memory circuits may be controlled "by inputting a command" (Sukegawa et al teaches that in response to certain commands, memories may be made "active" or "inactive" for write and read operations--see column 28, lines 29-49, e.g.), but does not teach that the plurality of memory circuits are "provided in a memory chip."

Lee et al similarly discloses an electrically rewritable semiconductor memory device such as an EEPROM including a plurality of "memory circuits" which share a data bus, where writing operations in the plurality of memory circuits may be simultaneously carried out in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al further teaches that the plurality of memory circuits may be "provided in a memory chip" [see column 3, lines 15-17 and 55-58, and also see EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 4, line 50 to column 5, line 7, e.g.]. As those of ordinary skill in the art would readily appreciate, integrating a plurality of similar circuits on an integrated circuit (IC) or "chip" allows the overall size and cost of the circuit to be decreased, and also provides fewer interconnections, increasing reliability.

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to provide the plurality of EEPROM memory circuits in Sukegawa et al (U.S. '001) "in a chip," and to control the activity and inactivity of each of the

memory circuits "by inputting a command," as taught by Lee et al, in order to selectively allow certain memory arrays or circuits on the chip to be made "active" or "inactive" for read and write operations, and to obtain smaller overall size and cost and improved reliability, all highly desirable features in a semiconductor memory such as in Sukegawa et al (U.S. '001).

Since applicant's claims "read on" a structure and method rendered obvious to one of ordinary skill in the art by the combined teachings of the references, the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the prior art.

With respect to claim 6, a common chip enable terminal may be provided for the plurality of memory circuits in Lee et al since the activity and inactivity of the memory circuits may be selected by inputting a command, so that a common enable signal inputted to the chip enable terminal is supplied to a selected one of the memory circuits which has been selected by inputting the command, in order to provide a simply selection mechanism for the plurality of memory circuits which are provided on the same chip, as taught by Lee et al.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (U.S.'001) and Lee et al, taken together, as applied to claims 5 and 6 above, and further in view of Bruce et al.

Sukegawa et al ('001) in view of Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device, such as an electrically erasable programmable read only memory (EEPROM), including a plurality of "memory circuits," each having a ready/busy terminal as in

the claimed invention (see numbered paragraph 9 above, e.g.), but does not teach providing a common ready/busy signal terminal for the plurality of memory circuits, with the ready/busy state of a selected one of the memory circuits being output to a ready/busy signal terminal.

Bruce et al similarly discloses an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits, each having a ready/busy terminal, and also teaches providing a common ready/busy signal terminal for the plurality of memory circuits, with the ready/busy state of a selected one of the memory circuits being outputted to a ready/busy signal terminal. In this manner, the ready/busy state of all memory circuits in a "bank" or group may be easily monitored without polling the status of each of the memory circuits [see column 3, lines 19-32; column 9, lines 6-12; column 13, lines 20-21; and Figures 4 and 5, e.g.].

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to provide a common ready/busy signal terminal for a plurality of memory circuits, with the ready/busy state of a selected one of the memory circuits outputted to a ready/busy signal terminal, as taught by Bruce et al, in the nonvolatile memory including a plurality of memory circuits such as in Sukegawa et al (U.S. '001) and Lee et al, taken together, as previously discussed, in order to quickly and easily monitor the ready/busy states of the memory circuits.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

It is once again noted that the Information Disclosure Statement (IDS) filed September 6, 2002 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 and has NOT been considered because a translation of the relevant portions of the non-English language reference was not provided. The IDS has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 C(1).

[Note that while an English language abstract may sometimes satisfy the statement of relevance requirement for a non-English language publication, it is not sufficient here since the reference was cited in a Korean Office action (see page 1 of the IDS) and the abstract does not sufficiently explain the reference's relevance or why it was cited in the Korean Office action. A translation of the relevant portions of the Korean Office action should also be provided for proper consideration by the Examiner.]

12. Applicants' arguments filed June 16, 2003 have been considered but are not persuasive. It is believed applicants' arguments have been addressed in the preceding paragraphs.

With respect to claims 1 and 4, as well as claims 5-6 and 8, applicant's arguments appear to be directed to Sukegawa (U.S. '814), not Sukegawa et al (U.S. '001).

Also with respect to claims 5 and 6, while the response asserts that "claims 4-6 recite substantially the same limitation discussed above" with respect to claim 1 (response at page 22), claim 5 does not include most of the limitations of claim 1. Thus, the argument presented with respect to claim 5, as well as claim 6 dependent therefrom, is not commensurate in scope with the claim language.

13. Claims 13, 17 and 20, insofar as definite and clear, would appear to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187